Intel Corporation
4030 Lafayette Center Drive
Chantilly, VA 20151

Intel Legal Team

Fax

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Confidential

Date: August 5, 2004

To:	Fax:	Art Unit:
Examiner David A. Zarneke USPTO	(703) 872-9306	2827
From:	**Fax:**	**M/S:**
B. Delano Jordan	703-633-3303	

Subject: Electrical/Optical Integration Scheme Using Direct Copper Bonding
Application No.: 10/020,911; Inventor: Gilroy J. Vandentop, et al.
Filed: December 19, 2001 Docket No. P12665

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Serita Evans _____ Date: August 5, 2004

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Fax Cover Sheet (1 page)
Transmittal Form (1 page)
Fee Transmittal (1 page in duplicate)
Appeal Brief (10 pages submitted in triplicate)

PTO/SB/21 (08-03)
Approved for use through 09/30/2003. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/020,911
Filing Date	December 18, 2001
First Named Inventor	Glenn J. Vandentop
Art Unit	2827
Examiner Name	David A. Zarneke
Attorney Docket Number	42390P12665

Total Number of Pages in This Submission: 33

ENCLOSURES (Check all that apply)

- [ ] Fee Transmittal Form
- [ ] Fee Attached
- [ ] Amendment/Reply
- [ ] After Final
- [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
- [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) ____
- [ ] After Allowance communication to Technology Center (TC)
- [ ] Appeal Communication to Board of Appeals and Interferences
- [x] Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) (please identify below):

Fax Cover Sheet; Brief in Support of Appeal (9 pages in triplicate)

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	B. Delano Jordan, Reg. No. 43,698 Intel Americas
Signature	
Date	8/5/04

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Typed or printed name	Serita Evans
Signature	Serita Evans
Date	8/5/04

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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PTO/SB/17 (10-03)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 330.00

Complete if Known	
Application Number	10/020,911
Filing Date	December 18, 2001
First Named Inventor	Gilroy J. Vandentop
Examiner Name	David A. Zarneke
Art Unit	2827
Attorney Docket No.	42390P12665

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☑ Deposit Account:

Deposit Account Number: 50-0221

Deposit Account Name: Intel Corporation

The Director is authorized to: *(check all that apply)*

☑ Charge fee(s) indicated below ☑ Credit any overpayments

☑ Charge any additional fee(s) or any underpayment of fee(s)

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

	Extra Claims		Fee from below	Fee Paid
Total Claims		-20** =		x =
Independent Claims		- 3** =		x =
Multiple Dependent				=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1206	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	330.00
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify)

*Reduced by Basic Filing Fee Paid SUBTOTAL (3) ($) 330.00

SUBMITTED BY

(Complete if applicable)

Name (Print/Type)	B. Delano Jordan	Registration No. (Attorney/Agent) 43,698	Telephone 703-633-0952
Signature		Date	8/5/04

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PTO/SB/17 (10-03)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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Complete if Known	
Application Number	10/020,811
Filing Date	December 19, 2001
First Named Inventor	Gilroy J. Vandentop
Examiner Name	David A. Zarneke
Art Unit	2827
Attorney Docket No.	42390P12865

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☑ Charge any additional fee(s) or any underpayment of fee(s)

☐ Charge fee(s) indicated below, except for the filing fee

to the above-identified deposit account.

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SUBTOTAL (2) ($)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

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1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify)

*Reduced by Basic Filing Fee Paid SUBTOTAL (3) ($) 330.00

SUBMITTED BY					
Name (Print/Type)	B. Delano Jordan	Registration No. (Attorney/Agent)	43,695	Telephone	703-633-0962
Signature				Date	8/5/04

(Complete if applicable)

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P12665 *Patent*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:		
Gilroy J. Vandentop, et al.	Examiner:	Zarneke, David A.
Serial No.: 10/020,911	Art Unit:	2827
Filing Date: December 19, 2001		
For: ELECTRICAL/OPTICAL INTEGRATION SCHEME USING DIRECT COPPER BONDING		

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF UNDER 37 C.F.R. § 1.192

Dear Sir:

Appellants hereby submit this Brief in triplicate in support of Appellants' appeal from a final decision of the Examiner mailed April 6, 2004 in the above-referenced application. Appellants respectfully request consideration of this Appeal Brief by the Board of Patent Appeals and Interferences for allowance of the above-referenced application.

REAL PARTY IN INTEREST

The real party in interest is Intel Corporation, a Delaware Corporation having a principal place of business in Santa Clara, California.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, Appellants' legal representatives, or the assignee that will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

STATUS OF CLAIMS

The above-referenced application, as originally filed, contained 30 claims. In response to a restriction requirement, Appellants elected claims 1-16. The Examiner further constructively elected claims 1-4 and 14-16 on the grounds that claims 5-13 were considered to be directed to another species. During prosecution, Appellants added new claim 31. Claims 1-4, 14-16 and 31 stand rejected under 35 U.S.C. § 103(a) as being considered to be unpatentable over Appellants' allegedly admitted prior art in view of Fan et al., "Copper Wafer Bonding", Electrochemical and Solid State Letters 2(10), pp. 534-536, 1999.

The claims on appeal are claims 1-4, 14-16 and 31 referenced above. Claims 1 is an independent claim. Claims 2-4, 14-16 and 31 depend from and further limit claim 1.

STATUS OF AMENDMENTS

A response after final office action under 37 C.F.R. § 1.116 was filed on February 9, 2004. In the response after final office action, no claims were amended. As Appellants understand the Advisory Action mailed February 23,

2004, the response after final office action was not entered because the remarks were considered to require further search and/or consideration.

SUMMARY OF INVENTION

The invention defined by claims 1-4 and 14-16 is a method of fabricating an electro-optic semiconductor package. According to the invention as defined by these claims, the method includes providing an integrated circuit (IC) wafer having one or more contact pads, the IC contact pads being connected to an IC on the IC wafer. An intermediate wafer having one or more intermediate contact pads is also provided, where the intermediate contact pads are connected to an electro-optic arrangement on the intermediate wafer. The method provides for direct copper bonding the IC contact pads to adjacent intermediate contact pads, where the electro-optic semiconductor package results. (See e.g. FIG. 3, blocks 52, 54 and 56, and Specification, paragraphs [0019]-[0021]).

The invention defined by claim 31 is a method of fabricating an electro-optic semiconductor package. The method includes the features described in the preceding paragraph, with the additional limitation that the direct copper bonding enables optical losses associated with the electro-optic semiconductor package to be minimized. (See, e.g. FIG. 2, optical components 26, 28 and 30, and Specification, paragraph [0021]).

ISSUES

Whether claims 1-4, 14-16 and 31 are patentable under 35 U.S.C. § 103(a) over Appellants' allegedly admitted prior art and Fan et al., "Copper Wafer Bonding", Electrochemical and Solid State Letters 2(10), pp. 534-536, 1999 ("Fan").

GROUPING OF CLAIMS

Group I Claims 1-4 and 14-16 stand or fall together in Group I; and.

Group II Claim 31 stands and falls alone in Group II.

ARGUMENT

Claim 1 is patentable over Appellants' allegedly admitted prior art and Fan

Claims 1-4 and 14-16 have been rejected under 35 U.S.C. §103(a) over what has been described as "Applicant's admitted prior art" and Fan et al., "Copper Wafer Bonding", Electrochemical and Solid State Letters, 2(10), pp. 534 536, 1999. For purposes of discussion, it is assumed that "Applicant's admitted prior art" refers to paragraphs [0003]-[0005] of the present specification, in view of paragraph 2, page 5 of the Office Action.

To establish a prima facie case of obviousness under § 103, all claim limitations of a claimed invention must be taught or suggested by the prior art. See MPEP, Section 2143.03 and *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). In view of the foregoing authority, the Appellants respectfully

submit that the basis relied on by the Examiner for the asserted rejection does not establish a prima facie case of obviousness.

In particular, paragraphs [0003]-[0005] make no mention of direct copper bonding, a technique that prior to the present application, had been limited to electrical applications. The Office action (page 5, paragraph 5) acknowledges this shortcoming and relies upon Fan to provide the missing element. In particular, the Office Action alleges that the claimed feature "would have been obvious ... because Fan teaches that [with direct copper bonding] interconnect delays are significantly reduced and system performance is increased." The Office Action cites the first paragraph of Fan as support for this proposition.

However, it is noted that Fan, in the first paragraph thereof (and, indeed, throughout), refers only to the advantages derived by using direct copper bonding to connect electrical devices. There is nothing in Fan to suggest that similar advantages might be obtained by using direct copper bonding with optical devices.

In this connection, it is further noted that the CAFC has held that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Fritch*, 972 F.2d 1260, 1266 (Fed. Cir. 1992). Further, with regard to combining prior art teachings to contend that the combination renders a claimed invention obvious, the CAFC has held that "[t]here must be some reason, suggestion or motivation found in the prior art whereby a person of ordinary skill in the field of the invention would make the

combination. That knowledge cannot come from the applicant's invention itself." *In re Oetiker*, 977 F.2d 1443, 1447, 24 USPQ2d 1443, 1446 (Fed. Cir. 1991).

Here, the only source to be found for the alleged motivation to modify the electrical devices of Fan to arrive at the claimed invention is the Appellants's own disclosure. Absent this disclosure, the claimed invention is anything but obvious. Optical devices have been historically difficult to fabricate using silicon-based processes. Typically, processes for fabricating optical devices (e.g., lasers) and processes for fabricating semiconductor devices are incompatible, for example because the respective processes use different materials and because a step or steps in one process could compromise or damage a structure formed in the other process. Thus, integrating optical devices with semiconductor devices has presented long-standing challenges that the present invention addresses in a novel and non-obvious fashion.

It is further observed that the reliance of the Office Action on an argument citing "inherent properties" is misplaced. Specifically, the Office Action states: "[S]eeing as Fan teaches that direct copper bonding is a known in the art method, the optic advantages of using direct copper bonding would be inherent properties" (page 2, paragraph 5). As a threshold matter, it is observed that the meaning of this statement is unclear, for at least the reason that it appears to equate "optic advantages" with "inherent properties." What "advantages" and what "properties" are meant is not clear, and in any event an "advantage" is not a "property." Moreover, whatever is meant by "optic advantages" and "inherent properties," the statement does not bear on the asserted obviousness rejection

for at least the reason that, as discussed previously, there is no discussion whatsoever in Fan of optical devices.

Note is further taken of the statement in the Office Action that "[t]he use of old process steps employing new materials is unpatentable," citing *In re Maxwell and Landes*, 89 USPQ 387 (CCPA 1951). The Appellants respectfully submit that this statement, however it is believed to apply to the present application, is plainly contrary to the holding of *In re Maxwell*. In that case, the court held that the Appellants' use of a new resin developed by others in the making of paper was patentable.

In consideration of the foregoing, claim 1 is clearly allowable over the art of record. Moreover, because claims 2-4 and 14-16 depend on claim 1, they are likewise allowable for at least the reasons discussed in connection with claim 1. Withdrawal of the rejection of claims 1-4, 14-16 and 31 under 35 U.S.C. §103(a) is therefore respectfully requested.

Claim 31 is patentable over Appellants' allegedly admitted prior art and Fan

Claim 31 has also been rejected under 35 U.S.C. §103(a) over what has been described as "Applicant's admitted prior art" and Fan. Appellants respectfully assert that the allegedly admitted prior art and Fan fail to meet a prima facie case of obviousness because all of the claimed limitations are not taught or suggested by the references.

In particular, claim 31 recites that the direct copper bonding enables optical losses associated with the electro-optic semiconductor package to be

minimized. As already mentioned, Fan demonstrates no appreciation for optical losses or the usefulness of direct copper bonding in minimizing these losses. Indeed, Appellants assert that one of ordinary skill would not normally consider a purely electrical technique to provide advantages in the optical domain as claimed. Accordingly, the art can support no implicit motivation to modify Fan to minimize optical losses in an electro-optic semiconductor package. There must be an express suggestion to combine optics with direct copper bonding before a hypothetical worker would do so. For at least the above reasons, Appellants request that the Board reverse the rejection of claim 31.

SUMMARY

In summary, Appellants respectfully submit that all of the claims on appeal are patentable over the references cited in the Final Office Action, and respectfully request a favorable decision by the Board.

If there are any charges, please charge Deposit Account No. 50-0221.

Respectfully submitted,

Dated: 8/5, 2004

B. Delano Jordan
Registration No. 43,698
Intel Americas, Inc.
2200 Mission College Blvd.
Santa Clara, CA 95052-8119
(703) 633-3360

CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below

By: Sonia Evans Date: August 5, 2004

APPENDIX

Claims on Appeal

1. A method of fabricating an electro-optic semiconductor package, the method comprising:

providing an integrated circuit (IC) wafer having one or more IC contact pads, the IC contact pads being connected to an IC on the IC wafer;

providing an intermediate wafer having one or more intermediate contact pads, the intermediate contact pads being connected to an electro-optic arrangement on the intermediate wafer; and

direct copper bonding the IC contact pads to adjacent intermediate contact pads, the electro-optic semiconductor package resulting.

2. The method of claim 1 further including:

cleaning the contact pads;

disposing the IC contact pads adjacent to the intermediate contact pads in an oxidation-resistant environment having a predetermined ambient temperature; and

forcing the IC contact pads into direct contact with the adjacent intermediate contact pads at a predetermined pressure, a direct copper bond resulting.

3. The method of claim 2 further including cleaning the contact pads in an acid bath.

4. The method of claim 2 further including disposing the IC contact pads adjacent to the intermediate contact pads in a nitrogen environment.

14. The method of claim 1 further including providing a computer processor wafer having one or more IC contact pads.

15. The method of claim 1 further including providing a chip interposer as the intermediate wafer.

16. The method of claim 1 further including providing a host wafer as the intermediate wafer.

31. The method of claim 1, wherein the direct copper bonding enables optical losses associated with the electro-optic semiconductor package to be minimized.

P12665 *Patent*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Claims 1-4 and 14-16 have been rejected under 35 U.S.C. §103(a) over what has been described as "Applicant's admitted prior art" and Fan et al., "Copper Wafer Bonding", Electrochemical and Solid State Letters, 2(10), pp. 534 536, 1999. For purposes of discussion, it is assumed that "Applicant's admitted prior art" refers to paragraphs [0003]-[0005] of the present specification, in view of paragraph 2, page 5 of the Office Action.

To establish a prima facie case of obviousness under § 103, all claim limitations of a claimed invention must be taught or suggested by the prior art. See MPEP, Section 2143.03 and *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). In view of the foregoing authority, the Appellants respectfully

submit that the basis relied on by the Examiner for the asserted rejection does not establish a prima facie case of obviousness.

In particular, paragraphs [0003]-[0005] make no mention of direct copper bonding, a technique that prior to the present application, had been limited to electrical applications. The Office action (page 5, paragraph 5) acknowledges this shortcoming and relies upon Fan to provide the missing element. In particular, the Office Action alleges that the claimed feature "would have been obvious ... because Fan teaches that [with direct copper bonding] interconnect delays are significantly reduced and system performance is increased." The Office Action cites the first paragraph of Fan as support for this proposition.

However, it is noted that Fan, in the first paragraph thereof (and, indeed, throughout), refers only to the advantages derived by using direct copper bonding to connect electrical devices. There is nothing in Fan to suggest that similar advantages might be obtained by using direct copper bonding with optical devices.

In this connection, it is further noted that the CAFC has held that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Fritch*, 972 F.2d 1260, 1266 (Fed. Cir. 1992). Further, with regard to combining prior art teachings to contend that the combination renders a claimed invention obvious, the CAFC has held that "[t]here must be some reason, suggestion or motivation found in the prior art whereby a person of ordinary skill in the field of the invention would make the

combination. That knowledge cannot come from the applicant's invention itself." *In re Oetiker*, 977 F.2d 1443, 1447, 24 USPQ2d 1443, 1446 (Fed. Cir. 1991).

Here, the only source to be found for the alleged motivation to modify the electrical devices of Fan to arrive at the claimed invention is the Appellants's own disclosure. Absent this disclosure, the claimed invention is anything but obvious. Optical devices have been historically difficult to fabricate using silicon-based processes. Typically, processes for fabricating optical devices (e.g., lasers) and processes for fabricating semiconductor devices are incompatible, for example because the respective processes use different materials and because a step or steps in one process could compromise or damage a structure formed in the other process. Thus, integrating optical devices with semiconductor devices has presented long-standing challenges that the present invention addresses in a novel and non-obvious fashion.

It is further observed that the reliance of the Office Action on an argument citing "inherent properties" is misplaced. Specifically, the Office Action states: "[S]eeing as Fan teaches that direct copper bonding is a known in the art method, the optic advantages of using direct copper bonding would be inherent properties" (page 2, paragraph 5). As a threshold matter, it is observed that the meaning of this statement is unclear, for at least the reason that it appears to equate "optic advantages" with "inherent properties." What "advantages" and what "properties" are meant is not clear, and in any event an "advantage" is not a "property." Moreover, whatever is meant by "optic advantages" and "inherent properties," the statement does not bear on the asserted obviousness rejection

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Note is further taken of the statement in the Office Action that "[t]he use of old process steps employing new materials is unpatentable," citing *In re Maxwell and Landes*, 89 USPQ 387 (CCPA 1951). The Appellants respectfully submit that this statement, however it is believed to apply to the present application, is plainly contrary to the holding of *In re Maxwell*. In that case, the court held that the Appellants' use of a new resin developed by others in the making of paper was patentable.

In consideration of the foregoing, claim 1 is clearly allowable over the art of record. Moreover, because claims 2-4 and 14-16 depend on claim 1, they are likewise allowable for at least the reasons discussed in connection with claim 1. Withdrawal of the rejection of claims 1-4, 14-16 and 31 under 35 U.S.C. §103(a) is therefore respectfully requested.

Claim 31 is patentable over Appellants' allegedly admitted prior art and Fan

Claim 31 has also been rejected under 35 U.S.C. §103(a) over what has been described as "Applicant's admitted prior art" and Fan. Appellants respectfully assert that the allegedly admitted prior art and Fan fail to meet a prima facie case of obviousness because all of the claimed limitations are not taught or suggested by the references.

In particular, claim 31 recites that the direct copper bonding enables optical losses associated with the electro-optic semiconductor package to be

minimized. As already mentioned, Fan demonstrates no appreciation for optical losses or the usefulness of direct copper bonding in minimizing these losses. Indeed, Appellants assert that one of ordinary skill would not normally consider a purely electrical technique to provide advantages in the optical domain as claimed. Accordingly, the art can support no implicit motivation to modify Fan to minimize optical losses in an electro-optic semiconductor package. There must be an express suggestion to combine optics with direct copper bonding before a hypothetical worker would do so. For at least the above reasons, Appellants request that the Board reverse the rejection of claim 31.

SUMMARY

In summary, Appellants respectfully submit that all of the claims on appeal are patentable over the references cited in the Final Office Action, and respectfully request a favorable decision by the Board.

If there are any charges, please charge Deposit Account No. 50-0221.

Respectfully submitted,

Dated: 8/5, 2004

B. Delano Jordan
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Intel Americas, Inc.
2200 Mission College Blvd.
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CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below

By: Sonya Evans Date: August 5, 2004

APPENDIX

Claims on Appeal

1. A method of fabricating an electro-optic semiconductor package, the method comprising:

providing an integrated circuit (IC) wafer having one or more IC contact pads, the IC contact pads being connected to an IC on the IC wafer;

providing an intermediate wafer having one or more intermediate contact pads, the intermediate contact pads being connected to an electro-optic arrangement on the intermediate wafer; and

direct copper bonding the IC contact pads to adjacent intermediate contact pads, the electro-optic semiconductor package resulting.

2. The method of claim 1 further including:

cleaning the contact pads;

disposing the IC contact pads adjacent to the intermediate contact pads in an oxidation-resistant environment having a predetermined ambient temperature; and

forcing the IC contact pads into direct contact with the adjacent intermediate contact pads at a predetermined pressure, a direct copper bond resulting.

3. The method of claim 2 further including cleaning the contact pads in an acid bath.

4. The method of claim 2 further including disposing the IC contact pads adjacent to the intermediate contact pads in a nitrogen environment.

14. The method of claim 1 further including providing a computer processor wafer having one or more IC contact pads.

15. The method of claim 1 further including providing a chip interposer as the intermediate wafer.

16. The method of claim 1 further including providing a host wafer as the intermediate wafer.

31. The method of claim 1, wherein the direct copper bonding enables optical losses associated with the electro-optic semiconductor package to be minimized.

P12665 *Patent*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Gilroy J. Vandentop, et al.	Examiner:	Zarneke, David A.
Serial No.: 10/020,911	Art Unit:	2827
Filing Date: December 19, 2001		
For: ELECTRICAL/OPTICAL INTEGRATION SCHEME USING DIRECT COPPER BONDING		

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF UNDER 37 C.F.R. § 1.192

Dear Sir:

Appellants hereby submit this Brief in triplicate in support of Appellants' appeal from a final decision of the Examiner mailed April 6, 2004 in the above-referenced application. Appellants respectfully request consideration of this Appeal Brief by the Board of Patent Appeals and Interferences for allowance of the above-referenced application.

REAL PARTY IN INTEREST

The real party in interest is Intel Corporation, a Delaware Corporation having a principal place of business in Santa Clara, California.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, Appellants' legal representatives, or the assignee that will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

STATUS OF CLAIMS

The above-referenced application, as originally filed, contained 30 claims. In response to a restriction requirement, Appellants elected claims 1-16. The Examiner further constructively elected claims 1-4 and 14-16 on the grounds that claims 5-13 were considered to be directed to another species. During prosecution, Appellants added new claim 31. Claims 1-4, 14-16 and 31 stand rejected under 35 U.S.C. § 103(a) as being considered to be unpatentable over Appellants' allegedly admitted prior art in view of Fan et al., "Copper Wafer Bonding", Electrochemical and Solid State Letters 2(10), pp. 534-536, 1999.

The claims on appeal are claims 1-4, 14-16 and 31 referenced above. Claims 1 is an independent claim. Claims 2-4, 14-16 and 31 depend from and further limit claim 1.

STATUS OF AMENDMENTS

A response after final office action under 37 C.F.R. § 1.116 was filed on February 9, 2004. In the response after final office action, no claims were amended. As Appellants understand the Advisory Action mailed February 23,

2004, the response after final office action was not entered because the remarks were considered to require further search and/or consideration.

SUMMARY OF INVENTION

The invention defined by claims 1-4 and 14-16 is a method of fabricating an electro-optic semiconductor package. According to the invention as defined by these claims, the method includes providing an integrated circuit (IC) wafer having one or more contact pads, the IC contact pads being connected to an IC on the IC wafer. An intermediate wafer having one or more intermediate contact pads is also provided, where the intermediate contact pads are connected to an electro-optic arrangement on the intermediate wafer. The method provides for direct copper bonding the IC contact pads to adjacent intermediate contact pads, where the electro-optic semiconductor package results. (See e.g. FIG. 3, blocks 52, 54 and 56, and Specification, paragraphs [0019]-[0021]).

The invention defined by claim 31 is a method of fabricating an electro-optic semiconductor package. The method includes the features described in the preceding paragraph, with the additional limitation that the direct copper bonding enables optical losses associated with the electro-optic semiconductor package to be minimized. (See, e.g. FIG. 2, optical components 26, 28 and 30, and Specification, paragraph [0021]).

ISSUES

Whether claims 1-4, 14-16 and 31 are patentable under 35 U.S.C. § 103(a) over Appellants' allegedly admitted prior art and Fan et al., "Copper Wafer Bonding", Electrochemical and Solid State Letters 2(10), pp. 534-536, 1999 ("Fan").

GROUPING OF CLAIMS

Group I Claims 1-4 and 14-16 stand or fall together in Group I; and.

Group II Claim 31 stands and falls alone in Group II.

ARGUMENT

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By: _____ Date: August 5, 2004
Serita Evans

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